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PTO/SB/08A (08-03)

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Application Number	10/762,181
Filing Date	January 21, 2004
First Named Inventor	Mohklesi
Art Unit	2827
Examiner Name	Huan Huang
Attorney Docket Number	SAND-01021US0

U. S. PATENT DOCUMENTS

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Examiner Signature	huan huan g	Date Considered	10/27/05
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Substitute for form 1449/PTO <h2 style="text-align: center; margin: 0;">INFORMATION DISCLOSURE STATEMENT BY APPLICANT</h2> <p style="text-align: center; font-size: small;">(Use as many sheets as necessary)</p>	<h3 style="text-align: center; margin: 0;">Complete if Known</h3> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Application Number</td> <td>10/762,181</td> </tr> <tr> <td>Filing Date</td> <td>January 21, 2004</td> </tr> <tr> <td>First Named Inventor</td> <td>Mohklesi</td> </tr> <tr> <td>Art Unit</td> <td>2827</td> </tr> <tr> <td>Examiner Name</td> <td>Huan Huang</td> </tr> <tr> <td>Attorney Docket Number</td> <td>SAND-01021US0</td> </tr> </table>	Application Number	10/762,181	Filing Date	January 21, 2004	First Named Inventor	Mohklesi	Art Unit	2827	Examiner Name	Huan Huang	Attorney Docket Number	SAND-01021US0
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Sheet <u>2</u> of <u>5</u>													

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
HJ		US- 6222762	4/24/2001	Guterman et al.	
		US- 6246607	6/12/2001	Mang et al.	
		US- 6461905	10/8/2002	Wang et al.	
		US- 6617639	9/9/2003	Wang et al.	
HJ		US- 6642066	11/4/2003	Halliyal et al.	
		US- 2003/0002348	1/2/2003	Chen et al.	
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FOREIGN PATENT DOCUMENTS					
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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			

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Substitute for form 1448/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/762,181
		Filing Date	January 21, 2004
		First Named Inventor	Mohklesi
		Art Unit	2827
		Examiner Name	Ihuan Hoang
		Attorney Docket Number	SAND-01021US0
Sheet	3	of	5

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
HH	1	BORSON, et al., "Direct Measurement of the Energy Distribution of Hot Electrons in Silicon Dioxide," J. Appl. Phys., Vol. 58, No. 3.1, August 1985, pp. 1302-1313	
		BROWN, et al., "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide to Understanding and Using NVSM Devices," IEEE, pp. 198-200	
		CAMM, et al., "Engineering Ultra-Shallow Junctions Using IRTP™," IEEE, Vortek Industries Limited, 2002	
		CHAN, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," IEEE Electron Device Letters, Vol. EDL-8, No. 3, March 1987, pp. 93-95	
		CHOI, et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling-Down and Zero Program Disturbance," IEEE Symposium on VLSI Technology Digest of Technical Papers, 1996, pp. 238-239	
		CHOI, et al., "A Triple Polysilicon Stacked Flash Memory Cell With Wordline Self-Boosting Programming", IEEE, 1997, pp. 283-286	
		DIJKSTRA, et al., "ISSG RTO (In-situ Steam Generation Rapid Thermal Oxidation) Grown Tunnel Oxide for Improved Reliability of Flash Memories," Philips Semiconductors, pp. 85-86	
		DIMARIA, "Graded or Stepped Energy Band-Gap-Insulator MIS Structures (GI-MIS or SI-MIS)," American Institute of Physics, September 1979, pp. 5826-5828	
		DIMARIA, et al., "Dual-Electron-Injector-Structure Electrically Alterable Read-Only-Memory Modeling Studies," IEEE Transactions on Electron Devices, Vol. ED-28, No. 9, September 1981, pp. 1047-1053	
		DIMARIA, et al., "Electrically-Alterable Memory Using A Dual Electron Injector Structure," IEEE Electron Device Letters, Vol. EDL-1, No. 9, September 1980, pp. 179-180	

Examiner Signature	Ihuan Hoang	Date Considered	10/27/05
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		Art Unit	2827
		Examiner Name	Huan Hoang
Sheet 4 of 5	Attorney Docket Number	SAND-01021USO	

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Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
✓		DIMARIA, et al., "Extended Cyclability in Electrically-Alterable Read-Only-Memories," IEEE ELECTRON DEVICE LETTERS, VOL. EDL-3, NO. 7, July 1982, pp. 191-195	
		HIRAYAMA, et al., "Low-Temperature Growth of High-Integrity Silicon Oxide Films by Oxygen Radical Generated in High-Density Krypton Plasma," IEEE, 1999, pp. 10.3.1-10.3.4	
		KIM, et al., "Fast Parallel Programming of Multi-Level NAND Flash Memory Cells Using the Booster-Line Technology", Symposium on VLSI Technology Digest of Technical Papers, 1997, pp. 65-66	
		KONSTANTIN, et al. "Riding the Crest of a New Wave in Memory, NOVORAM: A new Concept for Fast, Bit-Addressable Nonvolatile Memory Based on Crested Barriers," Circuits and Devices, July 2000, p. 17	
		KOTECHA, et al., "WAM 3.2: A Dual-Gate Floating Gate FET Device," IEEE International Solid-State Circuits Conference, 1981, pp. 38-39	
		KOROTKOV, et al., "Resonant Fowler-Nordheim Tunneling through Layered Tunnel Barriers and its Possible Applications," 1999 IEEE, 0-7803-5413-3/99	
		LEE, et. al., "Effects of Floating Gate Interference on NAND Flash Memory Cell Operation," IEEE Electron Device Letters, Vol. 23, No. 5, May 2002, p. 264	
		NOZAKI, et al., "A 1-Mb EEPROM With NONOS Memory Cell for Semiconductor Disk Application," IEEE Journal of Solid-State Circuits, Vol. 28, No. 4, April 1991, pp. 497-501	
		OHMI, et al., "New Paradigm of Silicon Technology," Proceedings of the IEEE, Vol. 89, No. 3, March 2001, pp. 394-412	
✓		OHTSUBO, et al., "Low Temperature Growth (400°C) of High-Integrity Thin Silicon-Oxynitride Films by Microwave-Excited high-Density Kr/O2/NH3 Plasma," pp. 166-169	

Examiner Signature	Huan Hoang	Date Considered	10/27/05
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		First Named Inventor	Mohklesi
		Art Unit	2827
		Examiner Name	Huan Huang
Sheet 5 of 5	Attorney Docket Number	SAND-01021US0	

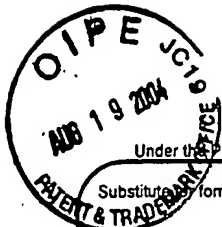
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HU		SATO, et al., "A Novel Channel Boost Capacitance (CBC) Cell Technology with Low Program Disturbance Suitable for Fast Programming 4Gbit NAND Flash Memories", IEEE Symposium on VLSI Technology Digest of Technical Papers, 1998, pp. 108-109	
		SATO, et al., "A Novel Gate-Offset NAND Cell (GOC-NAND) Technology Suitable for High-Density and Low-Voltage-Operation Flash Memories," Technical Digest of 1999 IEDM, section 11, number 2, p. 275	
		SEIDEL, et al., "Progress and Challenges for ALD Applications," Genus, Inc., August 5, 2003, pp. 1-39	
		SEKINE, et al., "Highly Reliable Ultrathin Silicon Oxide Film Formation at Low Temperature by Oxygen Radical Generated in High Density Krypton Plasma," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pp. 1550-1555	
		SUH, et al., "A 3.3V 32 Mb NAND Flash Memory With Incremental Step Pulse Programming Scheme," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, February 1995, pp. 94-95, 305-306, 128-129, and 350	
HU		YU, et al., "Energy gap and band alignment for (HfO ₂) _x (Al ₂ O ₃) _{1-x} on (100) Si," Applied Physics Letters, Volume 81, Number 2, July 8, 2002, pp. 376-378	

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Sheet 1 of 1

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HH		BUCKLEY, et al., "Engineering of 'Conduction Band-Crested Barriers' or 'Dielectric Constant-Crested Barriers' in view of their application to floating-gate non-volatile memory devices," pp. 55-56.	

Examiner Signature	Huan Huan	Date Considered	10/27/05
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First Named Inventor	Mohklesi
Art Unit	2818-2827
Examiner Name	Ileana Hwang
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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
EW		EP 0105802	4/18/1984	Fairchild Camera & Instrument Corporation		
WJH		JP 59147461	8/23/1984	Seiko Instr & Electronics Ltd		

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